REMARKS

Claims 1, 2, and 5-14 are presently under consideration. Claims 3 and 4 have been previously withdrawn from consideration. Favorable reconsideration of the subject patent application is respectfully requested in view of the comments made herein.

I. Rejection of Claims 1, 2, and 5-14 Under 35 U.S.C. §102(e)

Claims 1, 2, and 5-14 are rejected under 35 U.S.C. §102(e) as being anticipated by Nakajima *et al.* (U.S. 5,329,482). Applicants' representative respectfully submits that it should be withdrawn for at least the following reasons. Nakajima, *et al.* does not disclose each and every element recited in the respective claims.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). That is, the identical invention must be shown in as complete detail as is contained in the ... claim. *See Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Examiner continues to assert that Nakajima *et al.* discloses "forming source and drain regions of MOS transistors of a memory cell section and a peripheral circuit section formed on one and the same substrate (Column 2, lines 66-67, and Column 3, lines 20-23, 38-41), therefore achieving doping of adjacent polysilicon lines in the same area, adjacent polysilicon lines with space between them and polysilicon lines in the core area and in the peripheral area." (Paper no. 15, p. 2). For additional support of her argument, the Examiner cites to Column 1, lines 29-33 and 41-43, for the assertion that "plural memory cells and peripheral circuit formation is recited for accessing the memory cells which is a disclosure of plural FETs in the peripheral area." Applicants respectfully disagree.

Apparently, it appears that the Examiner has misinterpreted the cited portions of Nakajima *et al.* by unduly broadening or altering the scope of its teachings. In the first instance (cited portions in columns 2 and 3), Nakajima *et al.* discloses that a (single) MOS transistor can be formed in each of the memory cell section and the peripheral circuit section as shown in Nakajima's Fig. 5. Contrary to the Examiner's assertions, Nakajima *et al.* fails to disclose, teach or suggest depositing a first oxide layer over at least ***two adjacent polysilicon lines in each of a core area and a periphery***

area...implanting an area located between at *least two adjacent polysilicon lines in the core area*...the core area retaining an amount of the second oxide *between the adjacent polysilicon lines* while the periphery area is deplete of the second oxide *between its adjacent polysilicon lines* – as claimed in the subject application. On its face, Nakajima *et al.* does not teach each and every element as claimed and recited herein.

The claimed invention relates to a method of fabricating dual insulating spacers located adjacent to plural polysilicon lines in each of a nonvolatile memory cell and its peripheral circuitry. Claim 1 of the present invention recites depositing a first oxide layer over at least *two adjacent polysilicon lines in each of a core area and a periphery area*...implanting an area located between at *least two adjacent polysilicon lines in the core area*...the core area retaining an amount of the second oxide *between the adjacent polysilicon lines* while the periphery area is deplete of the second oxide *between its adjacent polysilicon lines*. Independent claims 5 and 13 recite similar limitations. It is clear from the specification of the present invention that "area" is intended to mean two distinct locations: *the core area and the periphery area. See, e.g.*, page 1, line 10. Furthermore, independent claim 1 requires a single implantation step, which occurs *between adjacent polysilicon lines in the core area*, after the first spacer etch, but before formation of the second spacer (oxide layer).

Hence, on its face, Nakajima *et al.* plainly does not disclose ***each and every element*** of the claimed invention. Furthermore, Figure 5 of Nakajima *et al.* explicitly shows a single polysilicon line in a core area and a single polysilicon line in a peripheral area. Put another way, these single polysilicon lines are in each of a core region and a peripheral circuit region. In fact, the core region is isolated or delimited from the peripheral region. *See* Column 5, lines 12-19. Thus, it is clear that the two lines are NOT in the same area according to the teachings of Nakajima, but rather are expressly described as being in two separate and distinct regions/areas of the substrate.

Since Nakajima *et al.* fails to teach adjacent polysilicon lines in the same area, it necessarily fails to disclose doping of adjacent polysilicon lines in the same area. The forming of source and drain regions *via* doping of regions surrounding a gate merely creates a gradient to effect potential current flow from the source to the drain. Thus, Nakajima *et al.*'s disclosure of *doping both sides of a single polysilicon line* is distinguishable and different from doping *between* adjacent polysilicon lines in the same area in order to form sources and drains.

In the second instance (cited portions in column 1), Nakajima's disclosure that "a memory section consisting in a matrix array of a large number of memory cells and a peripheral circuit section for controlling data input and output ..." does not teach and/or anticipate depositing a first oxide layer over at least *two adjacent polysilicon lines in each of a core area and a periphery area*...implanting an area located between at *least two adjacent polysilicon lines in the core area*...the core area retaining an amount of the second oxide *between the adjacent polysilicon lines* while the periphery area is deplete of the second oxide *between its adjacent polysilicon lines* – as claimed in the subject application. Again, Applicants respectfully contend that the Examiner is unduly broadening or altering the scope of Nakajima *et al.* The cited portions of column 1 as well as of columns 2 and 3, or any other portion, of Nakajima *et al.* plainly do not teach each and every element of the claimed invention.

Furthermore, in the Final Office Action (Paper no. 13), the Examiner appeared to contend that forming source and drain regions of MOS transistors of a memory cell section (core) and a peripheral circuit section (periphery) on one and the same substrate achieves doping of adjacent polysilicon lines in the same area, adjacent polysilicon lines with space between them and polysilicon lines in the core area and in the peripheral area, and thus anticipates the present invention. Applicants' respectfully disagree.

According to the teachings of Nakajima *et al.* and the Examiner's own argument (*see* Paper no. 13), two separate regions/areas are formed on the Nakajima *et al.* substrate: a memory cell section and a peripheral circuit region. Thus, these two separate regions are not equivalent and cannot be considered as one. Instead, each is defined by independent characteristics and properties as reflected by at least their two different names, features, and locations on the substrate.

Moreover, it would be highly improper to assert that the memory cell section constitutes the same area as the peripheral circuit region or vice versa. More specifically, it would be highly improper to argue that a single polysilicon line is formed in both the memory cell region (core) and in the peripheral circuit region when such is not disclosed in Nakajima *et al.* Nakajima *et al.* teaches forming a single polysilicon line in the core and a single polysilicon line in the peripheral region. Contrary to the implications of the Examiner, these two regions located on one and the same substrate constitute distinct areas of the substrate.

Because Nakajima *et al.* fails to teach each and every element of the present invention, the subject application is not anticipated by Nakajima *et al.* Accordingly, this rejection should be withdrawn.

II. Conclusion

The present application is believed to be condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063.

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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